In the Claims:

Please amend claims 1 and 4-6 as indicated below. This listing of claims replaces all prior versions.

1. (Currently amended) An insulated gate field effect transistor, comprising:

a semiconductor body defining opposed first and second major surfaces;

a drain region of a first conductivity type extending vertically between the second major surface and part of the first major surface;

a body region of a second conductivity type opposite to the first conductivity type extending from the first major surface to a body depth;

a source region of the first conductivity type adjacent to the body region at the first major surface;

a source contact contacting the source region and a drain contact contacting the drain region, and

an insulated gate extending laterally over the first major surface over the body region, defining a channel region extending in the body region from a source end adjacent to the source region to a drain end adjacent to a ~~drain~~ channel end part of the drain region,

further comprising:

a conductive shield plate for shielding the gate, extending in an insulated trench from the first major surface towards the second major surface, the conductive shield plate being separated from the body region by part of the drain region including the channel end part of the drain region and the conductive shield plate being electrically connected to the source region.

2. (Previously presented) An insulated gate field effect transistor according to claim 1, further comprising

a conductive shield plate extension connected to the shield plate extending laterally over the first major surface of the drain region from the shield plate towards the

channel end part of the drain region, the shield plate extension being separated by insulator from the drain region.

3. (Previously presented) An insulated gate field effect transistor according to claim 2, wherein a gate insulator layer extends under both the gate and the shield plate extension.

4. (Currently amended) An insulated gate field effect transistor according to claim 2, wherein the lateral gap between the shield plate extension and the gate is in the range of about 0.05 to about 0.2 microns.

5. (Currently amended) An insulated gate field effect transistor according to claim 1, wherein the shield plate trench extends to a depth that is substantially equal to the body depth ~~is connected to the source~~.

6. (Currently amended) An insulated gate field effect transistor according to claim 1, wherein the depth of the shield plate trench is between about 50% and about 200% of the depth of the body region.

7. (Previously presented) An insulated gate field effect transistor according to claim 1, wherein the first conductivity type is n-type, the second conductivity type is p-type, and the shield plate is of p-type doped polysilicon.

8. (Previously presented) An insulated gate field effect transistor according to any preceding claim, wherein the lateral gap between the shield plate trench and the body region is between about 0.5 and about 2 microns.

9. (Previously presented) An insulated gate field effect transistor according to claim 1, wherein the gate extends over the channel end part of the drift region by no more than about 0.4 microns.